ENHANCEMENT IN POWER-DELAY PRODUCT BY DRIVER AND INTERCONNECT OPTIMIZATION

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Abstract

To obtain higher performance with maximum devices and smaller chip size semiconductor devices are continuously shrinking. However, leakage power dissipation increases significantly with the technology scaling. Increasing demand for ultra low power devices has increased significantly since last decade and it compels advance technological solutions to fulfill power requirements of electronic appliances. As a result subthreshold operation region and different device optimization techniques attracts different researchers to achieve ultra low power design of VLSI circuits. Power supply reduction is supposed to be the main parameter to reduce power reduction. However, deep subthreshold region offers speed penalty degrading the overall performance of a device which suggests the need for optimizing device parameters. This paper analyzes the driver and interconnects performance by changing threshold voltage (V_{th}) and oxide thickness (T_{ox}) in subthreshold region. Further, it also compares the optimized driver performance and DTMOS driver performance at 0.4 V. Moreover, a large amount of gain in performance was observed when optimized interconnect is used with the optimized driver. Result shows that performance of a circuit enhances if the optimized driver is used compared to DTMOS driver.

Keywords— *Driver; interconnect; PDP; repeater insertion; subthreshold region; threshold voltage.*

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1. INTRODUCTION

According to Moore's law, density of devices is continuously increasing on a chip. Technology scaling is being used to scale down the device dimensions in order to accommodate millions of transistors on a single small chip. However, interconnect performance degrades due to scaling of device beyond a particular limit which may degrade the signal transmission and it may become unfaithful. Thus, interconnects are becoming the limiting factor affecting circuit functionality such as speed, power and reliability. Interconnects, thus, have gained a significant attention as the performance of a circuit largely depends on the capability of interconnect to drive any signal around the circuit components. Furthermore, increasing demand of low power portable devices is also a key reason to make improvements in the interconnect designs and come up with the new techniques to satisfy the requirements of ULP applications [1][6]. Increasing demand of portable devices require very low power consumption. This demand for low power devices has given rise to subthreshold operation region.

One of the recent topics in VLSI today is to optimize the device, and/ or circuit, interconnect performance to satisfy the need of portable devices and also to extend the application domain of subthreshold circuits towards FPGAs. In subthreshold regime, subthreshold leakage current of a device is used as a drive current taking the benefit of low power consumption thereby increasing portability of electronic devices. However, speed penalty is a major drawback in this technique for which many researchers are working to find out a solution to minimize the overall delay. Device optimization changes the different parameters of a device to get optimum performance in subthreshold region keeping the lower bounds safe. Moreover, if the interconnect techniques are adopted along with the subthreshold operation, there is a possibility to get an enhanced performance of electronic devices in terms of both power and delay. Thus, it is necessary to put more efforts on both driver and interconnect design for low power application.

Interconnect dimensions also need to be scaled down along with the devices to gain the advantages obtained from device scaling. However, wires put a greater resistance with the decreasing wire width and increasing wire length. Further, interconnect capacitance and coupling capacitance limits the performance in deep nano scaled region exhibiting crosstalk between the densely placed interconnect wires which adversely affect the speed of wire. So, mitigating these barriers is of crucial importance in order to keep balance between the devices and interconnect performance. Authors have suggested different techniques to improve the performance of interconnect under superthreshold as well as subthreshold operating regions particularly for global interconnects as it decides the quality of signaling [1][4][6]. But, still the researchers are in search of some innovative and new ideas which will help to sustain technology scaling.

Interconnects have become the most important part of electronic circuits recently as the scaling of device dimensions has almost reached the yield point. Further scaling of device dimensions will bring the devices at atomic level where current conduction through these atomic devices is beyond imagination for now. Unlike devices, interconnects have scope for further scaling in subthreshold

region as the current density is very much less compared to current density in superthreshold. Number of interconnect optimization techniques has been proposed along with device's performance optimization techniques in superthreshold as well as subthreshold region to obtain the greater speed and low execution power of electronic appliances [1][2][5]. Some of the proposed techniques offer significant improvement in the speed of circuit at the cost of increased power consumption while some provide significant reduction in power consumption incurring penalty in speed [1][2]. But, under subthreshold region, these techniques do not perform as good as they do under superthreshold conditions. Thus, there is need to explore different techniques for subthreshold interconnects to get an optimum performance in speed and power as well. This section presents few techniques that already have been suggested for overall performance of a circuit considering both devices as well as interconnects.

Repeater insertion is a preferably used method for global interconnects under superthreshold operating region [1]. Low voltage operation is one of the promising techniques to enhance the power efficiency of nano scaled circuits. In subthreshold region, device optimization provides significant delay and PDP improvement when both the threshold voltage as well as oxide thickness is reduced to get optimum values of delay and PDP [1]. However, the total path delay can be reduced by varying interconnect geometrical parameters such as width, height and spacing. Further, some authors found 3D interconnects more suitable as these reduce the energy dissipation by 54% and propagation delay by 51% of long on-chip wires [3].

J. Kil et al. proposed a technique which involves boosting of a gate voltage to improve the speed and robustness which shifts the operating point of device from superthreshold to subthreshold region [4]. Further, O. Jamal and A. Naeemi suggested possible replacements for Cu such as SWCNT and GNR interconnects which also help in performance improvement of subthreshold circuits [5]. It was analyzed that compared to copper interconnects with a typical aspect ratio of 2, SWCNT and GNR interconnects are up to 4 times faster and dissipate up to 5 times less energy per switching operations. Y. Ho et al. investigated the performance of interconnects with repeater insertion in the subthreshold region [6]. Authors used high boosting predrivers which provide higher energy efficiency compared to the conventional repeaters. Though the above mentioned techniques definitely provide performance benefits, it is necessary to think about state-of-the-art technologies to bring a significant elevation in the speed of VLSI circuits.

Lot of work has been done and is still going on to use carbon nanotubes effectively as connecting material. Many have presented their analysis showing the possible benefits of carbon nanotubes which is helpful to improve the speed and power of electronic circuits. As CNTs exhibit extraordinary strength and unique electrical and mechanical properties these can be the possible solution for future interconnects. Though carbon nanotubes offer advantages over copper, their behavior as interconnect is not ideal. CNTs have high contact resistance due to imperfect metal nanotube contacts and are not suitable in superthreshold regions compared to the copper interconnects. In subthreshold region, instead, CNTs are the better option so far for short and intermediate interconnect as they bring significant decrease in the power consumption but speed penalty is the challenge. Currently, much focus is given on the speed improvement using carbon nanotubes as interconnects to overcome delay problem.

This paper mainly focuses on the performance improvement of interconnect considering several existing interconnect techniques and it incorporates some modifications in the traditional methods. Section I gives a brief introduction of the topic. Rest of the paper is organized as follows. Section II presents the effect and results of change in interconnect dimensions. Next, section III discusses the impact on performance of a device by optimizing the device parameters like V_{th} and T_{ox}. Section IV presents the DTMOS technique and its operation. Further, section V explores the performance of interconnects in the subthreshold operation region. Section VI focuses on results and analysis of proposed work. Section VII draws the conclusion.

2. INTERCONNECT PARAMETER OPTIMIZATION

Interconnect primarily determines the performance of the system at scaled technology node due to increase in chip size and slow scaling of interconnect dimensions compared to the active devices. Global interconnects and short interconnects need to be considered separately as they serve different functional areas and are placed according to the signals they carry. Global interconnects, for example, primarily are used for power supply and clock distribution while short and intermediate interconnects connect the two nearby transistors. Both the types of interconnects exhibit certain challenges with the continuously shrinking device size at each technology node.

The recent topic of research now a day is interconnect under subthreshold operating region as far as improvement in speed and power is concerned. Copper is being used as an interconnect material since past many years. With the scaling of technology node interconnects are also being scaled down which is gradually degrading the interconnect performance due to increased resistivity and electro-migration problem in strong operating region [7]. Optimization of interconnect parameters in superthreshold region degrades the performance while it offers improvement under subthreshold region. In this work, width (w) of interconnect is kept constant while height (h) and spacing (s) has been changed. Performance is measured with the help of a circuit consisting of a driver, interconnect, and receiver as shown in Fig.1.

For optimization of interconnect parameters power, delay, and PDP measurements at different supply voltages have been taken. In this paper, width of interconnect is kept

constant i.e. 48 nm while height and spacing is varied to observe mainly change in delay. This analysis has been done at three supply voltages for different values of height and spacing as shown in Fig. 2. From this plot it is clearly observed that a significant reduction can be obtained in PDP if the parameters are optimized at o.4 V i.e. under subthreshold region. Fig. 2 shows that minimum PDP is obtained if spacing is kept at 144 nm and height at 48 nm for comparatively shorter interconnect lengths, approximately up to 5mm. As the length moves beyond 5 mm better results are seen for height equal to 68nm instead of 48 nm. So, the optimized interconnect parameters according to results can be listed as height equal to 48 nm, spacing equal to 144 nm, and width being unchanged for interconnect length of up to 5 mm.

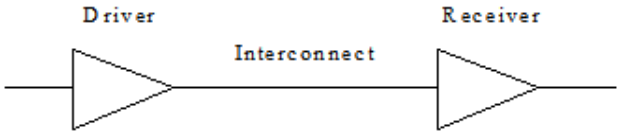

Fig.1. Simulation test bench

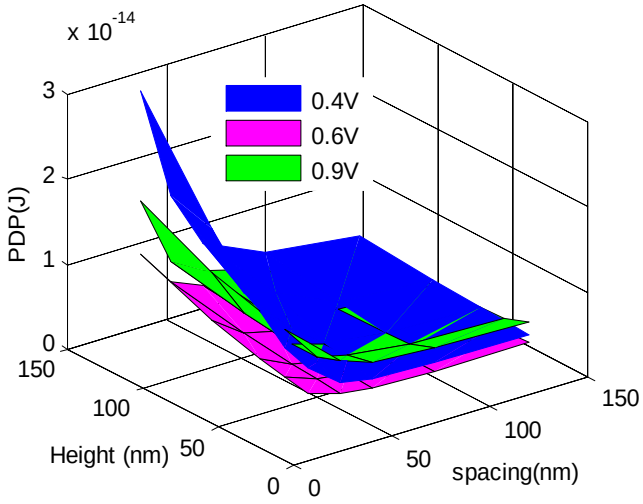

Fig.2 PDP measurement with varying spacing and height at different supply voltages

3. OPTIMIZATION OF DEVICE PARAMETERS

Demand for low power electronic devices has made subthreshold region of operation very essential in recent years. Though it offers a great advantage in power and performance of a circuit for short interconnects, long interconnects suffer from performance degradation due to increased driver resistance and interconnect capacitance. Conventional drivers that are designed to operate in superthreshold region do not provide optimum performance in subthreshold region [4][6]. Thus, to enhance the performance of a circuit and interconnect, device optimization can help overcome the problems in long interconnect under subthreshold condition.

Gate capacitance, static power dissipation, and gate leakage power dissipation are taken into consideration while optimizing devices in superthreshold region. These devices provide a penalty in speed under subthreshold region. Threshold voltage (V_{th}) has limits by the amount of subthreshold leakage current. The choice of V_{th} is a tradeoff between device speed and static leakage. As V_{th} is reduced, the term (V_{GS}-V_{th}) increases which shift the operating point of device towards moderate inversion region thereby increasing the drive current. Thus, lowering the threshold voltage increases the speed of a circuit in subthreshold region. Another important parameter to be considered is oxide thickness (T_{ox}) of a device which is necessary to keep the gate leakage current at minimum value in case of superthreshold region. Downscaling of T_{ox} causes lowering of S i.e. inverse subthreshold slope which degrades I_{ON}/I_{OFF} ratio. But, reduction of T_{ox} under subthreshold region does not increase gate leakage current due to lower supply voltage. The inverse subthreshold slope is given as:

$$S = 2.3V_T\left[1+\frac{3T_{ox}}{W_{dep}}\right]\left[1+\frac{11T_{ox}}{W_{dep}}e^{\left[\frac{-\pi l_{eff}}{2\left(W_{dep}+3T_{ox}\right)}\right]}\right] \quad \ldots\ldots(1)$$

Where W_{dep} is the depletion width, L_{eff} is the effective channel length, V_T is the thermal voltage and T_{ox} is the oxide thickness.

4. DTMOS TECHNIQUE

The proved and most common technique of power reduction is power supply scaling as the power delivered to the CMOS circuits is proportional to the square of the supply voltage as given below in Eq.

$$P = C_L V^2{}_{dd} f_d \quad \ldots\ldots\ldots\ldots\ldots\ldots(2)$$

Where C_L is the total switching capacitance, V_{dd} is the supply voltage, and f_d is the cooperating frequency of the gate. But, power supply reduction below threshold voltage degrades the speed significantly. Therefore, threshold voltage should also be reduced along with the power supply. Dynamic threshold MOS are used to scale the supply voltage beyond lower limit for low power operation. DTMOS has high V_{th} at zero bias and low V_{th} at V_{gs}=V_{dd}.

A strong barrier of performance improvement in subthreshold region is speed penalty. This technique makes a minor change in the conventional device i.e. body is connected to gate terminal instead of source. In this device, the threshold voltage of the device is a function of its gate voltage, i.e., as the gate voltage increases the threshold voltage (Vth) drops resulting in a much higher current drive than standard MOSFET for low-power supply voltages. On the other hand, Vth is high at Vgs = 0, therefore the leakage current is low. This way driver performance increases ultimately reducing the delay. However, triple well process is required for the implementation purpose of this device.

5. PERFORMANCE UNDER SUBTHRESHOLD DOMAIN

In subthreshold region, power consumption is reduced significantly by reduction in the supply voltage below threshold voltage. Though this technique offers speed penalty, decrease in the energy consumption is to such an extent that it suppresses all the other challenges. So, low voltage operation is one of the promising techniques to enhance the power efficiency of the nano scaled circuits. Furthermore, in subthreshold region, device optimization provides significant delay and PDP improvement when both the threshold voltage as well as oxide thickness is reduced to get optimum values of delay and PDP [6]. However, the total path delay can be reduced by varying interconnect geometrical parameters such as width, height and spacing. The increase in spacing provides reduction in interconnect delay and path delay as well whereas reducing the height of interconnect gives considerable decrease in PDP. This decrease in PDP is mainly due to lowering of interconnect capacitance in subthreshold region though resistance increases by a small amount.

In subthreshold domain, supply voltage is below threshold voltage which implies that the device is off under subthreshold conditions. As driver or device is off, driver resistance is more compared to the interconnect resistance. However, leakage current is used as a drive current and it is given as below:

$$I_D = I_0 e^{\left(\frac{V_{GS}-V_{th}+\eta V_{DS}}{nV_T}\right)}\left(1-e^{-\frac{V_{DS}}{V_T}}\right) \qquad (3)$$

Where,

$$I_0 = \mu_0 C_{ox} W/L(n-1)V_T^2$$

V_T is the thermal voltage, n is the subthreshold slope factor ($n=1+C_d/C_{ox}$), C_d and C_{ox} are depletion and oxide capacitances respectively, and **η** is drain induced barrier lowering coefficient that causes an increase in subthreshold current with drain voltage in short channel MOSFET.

Device delay increases exponentially as V_{DD} scales down due to exponential behavior of subthreshold leakage current [1]. Moreover, global interconnect delay increases further as interconnect provides higher capacitance in subthreshold domain. Lot of research work had been carried out to reduce the delay of global interconnects using various techniques like repeater insertion, driver optimization, interconnect parameter optimization etc. under superthreshold region. However, the effectiveness of these techniques should be ensured under subthreshold region along with new techniques.

6. PERFORMANCE ANALYSIS AND RESULTS

Since the evolution of semiconductor devices, there has been a trend in increasing density of devices on a chip as specified by ITRS [7]. Devices are scaled down from micron to submicron to nanometer regime in order to place more number of devices on a single chip. In recent years, technology has reached a deep nanometer region providing extremely small devices due to increasing demand of high speed and ultra low power electronic gadgets. However, this shrinkage has placed lower bounds on further scaling of a device as leakage power is also increasing thereby exhibiting poor performance in terms of power dissipation. So, the major challenge is to reduce power dissipation of devices retaining speed and robustness. This can be achieved if the device is operated in subthreshold region i.e. if supply voltage V_{DD} is kept below the device threshold voltage V_{th}. Further, interconnects also need to be scaled along with the devices. In subthreshold operating region, driver resistance is dominant over interconnect resistance due to lower supply voltage. Hence, to obtain a high performance and low power circuits there is a need to go for driver optimization.

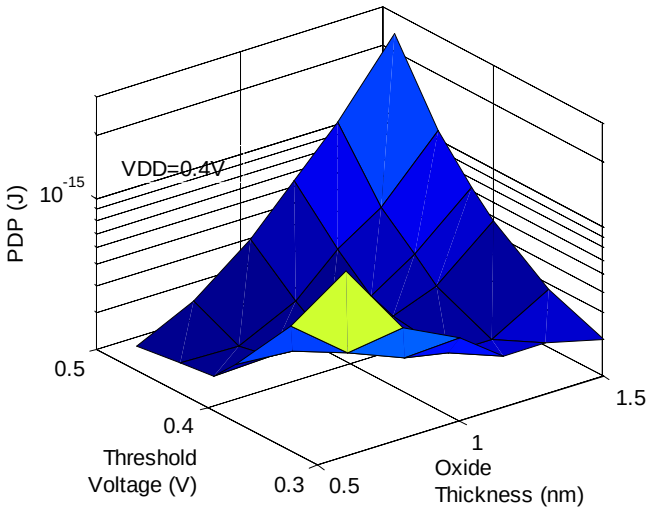

Fig.3.Effect of change in V_{th} and T_{ox} on PDP at 0.4V supply voltage.

In this work, two device parameters i.e. threshold voltage V_{th} and oxide thickness T_{ox} have been considered to get an optimum performance of a driver. To explore the power-delay tradeoff in subthreshold conditions, circuit as shown in Fig.1 is simulated for driver, interconnect, and a receiver delay. A CMOS inverter is used as a driver and receiver. At 32 nm HP technology node, threshold voltage and oxide thickness are defined as 0.49 V and 1.15nm respectively. As we move towards subthreshold region, supply voltage migrates below 0.49 V. In this paper, an analysis has been done by varying threshold voltage and oxide thickness. The improved results have been seen when V_{th} is kept at 0.42 V and oxide thickness is reduced from 1.15 nm to 1 nm. Compared to the conventional driver an optimized driver enhances speed by 3.2 times and the improvement in PDP is 3 times with only 5.5% penalty in power consumption. Fig. 3 shows the pattern of change in performance parameter of a driver by changing V_{th} and T_{ox} at 0.4 V V_{DD}. The curve is like a bathtub which shows fall in PDP initially after which

it obtains a minimum point and then again starts rising. Thus, values of V_{th} and T_{ox} are taken to be 0.42 V and 1 nm respectively which provide maximum improvement. In addition, improved interconnect parameters further increase the gain in speed and energy product. Interconnects with height as 144 nm and spacing between interconnects as 48 nm provide better performance compared to the conventional interconnect as shown in above

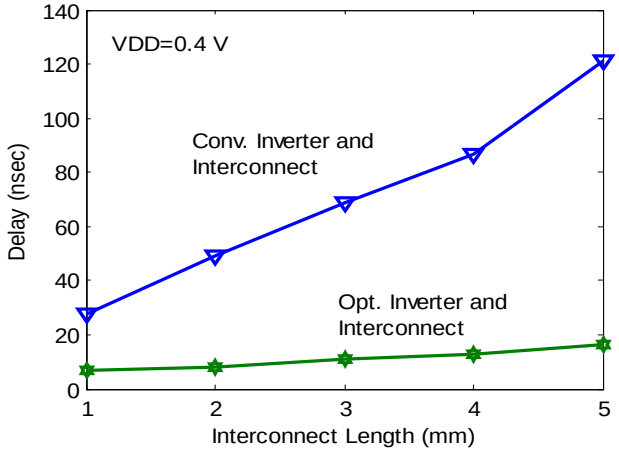

Fig.4. Change in delay for conv. Driver and opt. driver at 0.4 V supply voltage.

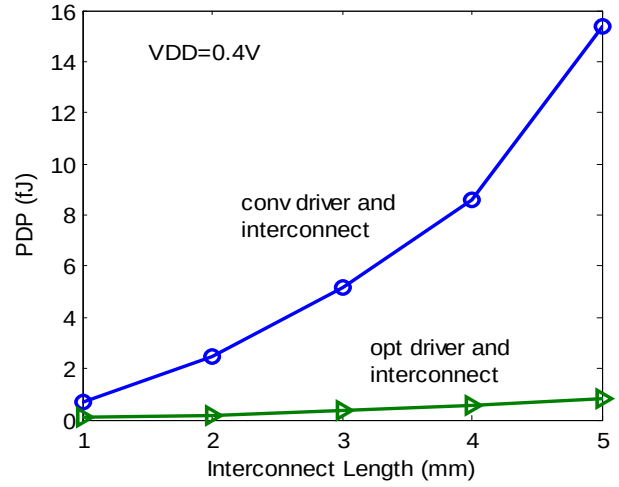

Fig.5. Change in PDP for conv. driver and opt. driver at 0.4 V supply voltage

Fig.2**.** Thus, interconnect with new interconnect parameters and driver with altered V_{th} and T_{ox} provide huge benefit in the overall performance. Fig.4 and Fig.5 clearly indicate the improvement in speed and PDP obtained by incorporating changes in both the device as well as interconnect respectively. Figures also specify that an increase in interconnect length adds to the better speed and PDP. From figures it can be observed that a conglomerate of an improved interconnect and driver achieves 4X and 7.9X improvement in speed and PDP respectively for 1 mm interconnect length and 7.5X and 18X improvement in speed and PDP respectively for 5 mm interconnect length. Moreover, power consumption also reduces by a considerable amount i.e. 2X for 1mm interconnect length and 2.5X for 5mm interconnect length. Static power consumption also plays a significant role under subthreshold region. This study extracts the performance of a driver in terms of static power dissipation and it has been found that there is 12 times rise in static power compared to the conventional driver. Though it increases static power dissipation, it is tolerable because the performance gain in terms of delay is dominant.

Furthermore, this paper also compares the performance of a driver and interconnects when a conventional CMOS device is replaced with the DTMOS device. DTMOS driver provides 1.3X improvement in PDP for 1 mm interconnect length and 2.4X for 5 mm interconnect length. Further, interconnect with improved interconnect dimensions with DTMOS driver offer even greater advantage compared to when only DTMOS driver is used with conventional interconnect parameters. This can be seen from Fig. 6 and Fig.7 that reduction in delay and PDP is by 2.7X and 3.1X respectively for 1 mm interconnect length and 4.6X and 9.8X for 5 mm interconnect length.

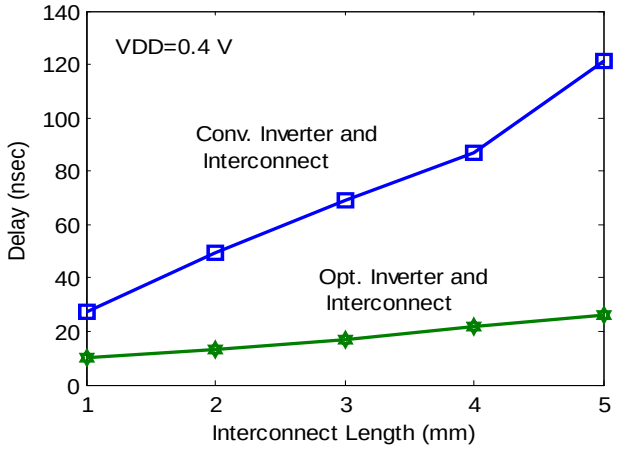

Fig.6 Change in delay for conv. driver and DTMOS driver at 0.4 V supply voltage.

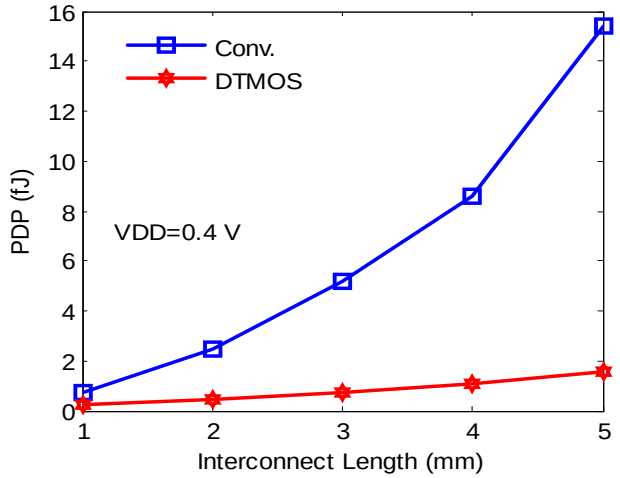

Fig.7. Change in PDP for conv. driver and DTMOS driver at 0.4 V supply voltage.

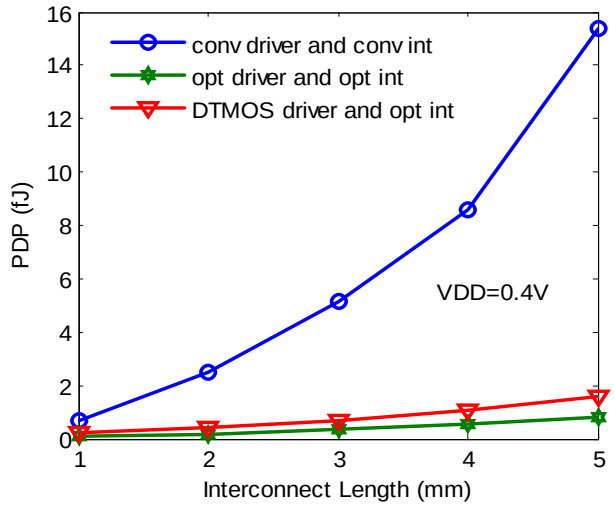

Fig.8. Comparison between performance of opt. driver and DTMOS driver with opt. interconnect

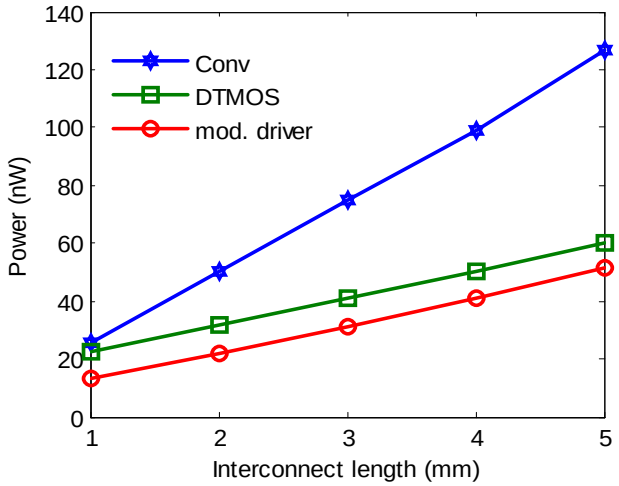

Fig.9. . Comparison between power consumption of opt. driver and DTMOS driver with opt. interconnect

Moreover, power consumption also reduces by 11% for 1 mm interconnect length and 52% for 5 mm interconnect which contributes to the improvement in PDP as shown in Fig.9.

The results and graphs conclude that for longer interconnect lengths the improvement in speed and PDP is more compared to shorter interconnects. Further, Fig.8 compares the PDP obtained by above test-bench with both DTMOS driver and improved interconnect as well as modified driver with respect to V_{th} and T_{ox} along with improved interconnect. The comparison of the three suggests a driver with altered V_{th} and T_{ox} as it provides the maximum improvement.

7. CONCLUSIONS

This paper has successfully carried out the simulation of a simple circuit consisting of a driver, receiver, and interconnect of different length from 1 mm to 5 mm considering different interconnect parameters than conventional under subthreshold conditions with supply voltage of 0.4 V. This paper mainly analyzed the results of a circuit by varying device parameters particularly V_{th} and T_{ox}. The new values of V_{th} and T_{ox} have been taken to be 0.42 V and 1 nm as these provide minimum delay and PDP. It also compared the performance by replacing a conventional device with a DTMOS device at the same supply voltage. Further, it has been observed that interconnect with increased spacing and reduced height gives better performance in terms of speed and PDP along with the change in device. Thus, integrating the interconnect having new parameters with altered device gave significantly better results than the conventional circuit. Analysis showed 18X improvement in PDP when a device with new device parameters had been used and 9.8X improvement in PDP when DTMOS device had been used for 5 mm interconnect length. Moreover, power consumption also reduced by a considerable amount i.e. 2.5X for a device with new V_{th} and T_{ox} values and 52% for DTMOS device. Hence, it can be concluded that performance of a circuit can be improved under subthreshold operating condition by incorporating changes in the device parameters.

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